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<Variant Name>



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KARNATAKA.

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Drawing Title
INDEX

Designer
Yash

Size
B

Scale

Document Number
CAVECSSCH00E00

Rev
0.1

Approved

Date : **Monday, September 13, 2021**

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1 of **16**

BLOCK DIAGRAM

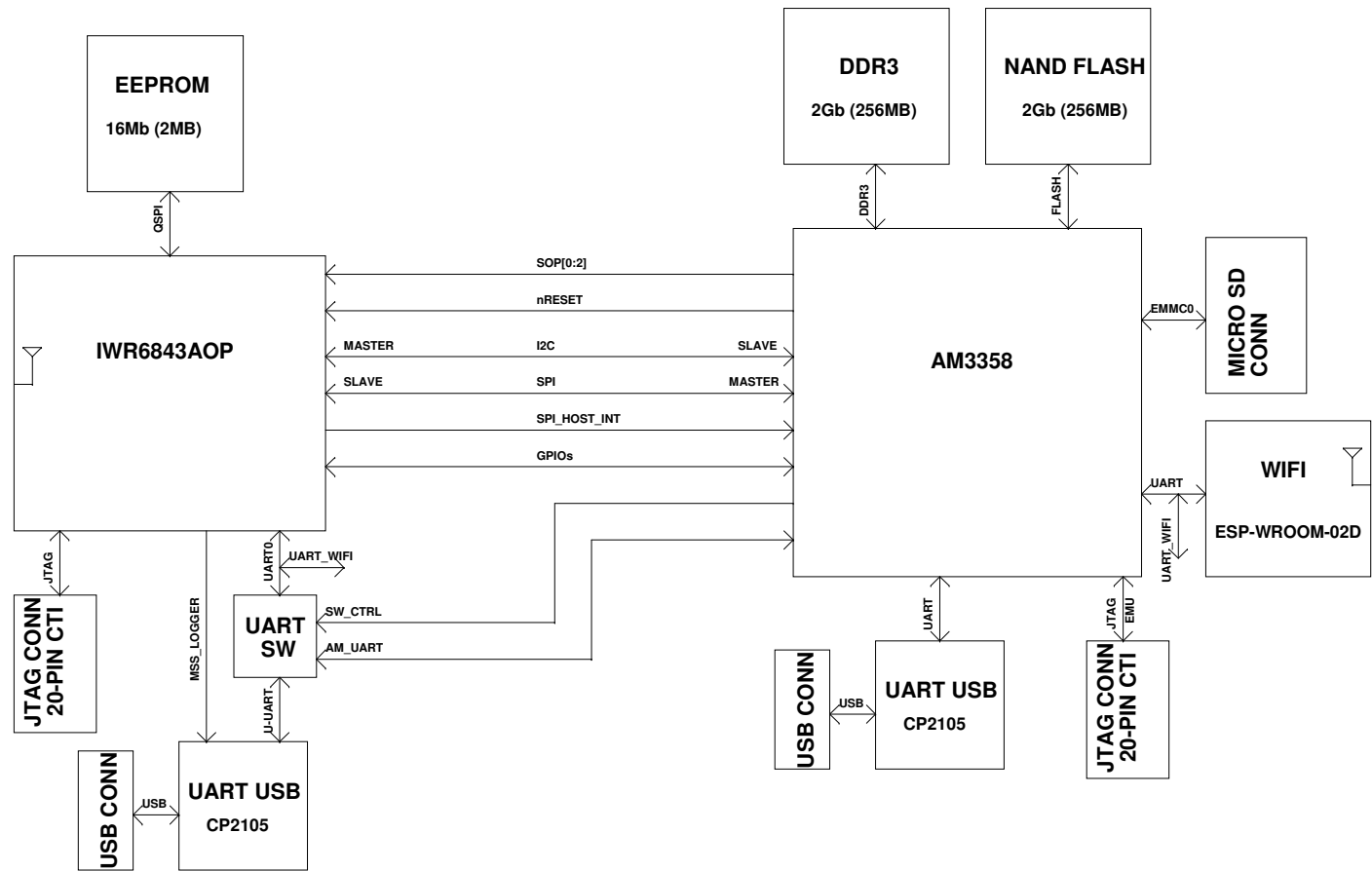
```
graph TD
    AM3358[AM3358]
    IWR6843AOP[IWR6843AOP]
    EEPROM[EEPROM 16Mb 2MB]
    DDR3[DDR3 2Gb 256MB]
    NAND_FLASH[NAND FLASH 2Gb 256MB]
    MICRO_SD_CONN[MICRO SD CONN]
    WIFI[WIFI ESP-WROOM-02D]
    JTAG_CT1_1[JTAG CONN 20-PIN CTI]
    USB_CT1_1[USB CONN]
    UART_SW[UART SW]
    UART_USB_1[UART USB CP2105]
    JTAG_CT1_2[JTAG CONN 20-PIN CTI]
    UART_USB_2[UART USB CP2105]

    AM3358 -- "SOP[0:2]" --> IWR6843AOP
    AM3358 -- "nRESET" --> IWR6843AOP
    IWR6843AOP -- "MASTER I2C SLAVE" --> AM3358
    IWR6843AOP -- "SLAVE SPI MASTER" --> AM3358
    IWR6843AOP -- "SPI_HOST_INT" --> AM3358
    IWR6843AOP -- "GPIOs" --> AM3358
    IWR6843AOP <--> |"QSPI"| EEPROM
    IWR6843AOP <--> |"JTAG"| JTAG_CT1_1
    IWR6843AOP <--> |"USB"| USB_CT1_1
    IWR6843AOP <--> |"UART WIFI"| UART_SW
    IWR6843AOP <--> |"SW_CTRL"| UART_SW
    IWR6843AOP <--> |"AM_UART"| UART_SW
    IWR6843AOP <--> |"UART"| UART_USB_1
    IWR6843AOP <--> |"JTAG EMU"| JTAG_CT1_2
    IWR6843AOP <--> |"USB"| UART_USB_2
    AM3358 <--> |"DDR3"| DDR3
    AM3358 <--> |"FLASH"| NAND_FLASH
    AM3358 <--> |"EMMC0"| MICRO_SD_CONN
    AM3358 <--> |"UART WIFI"| WIFI
    UART_SW <--> |"UART"| UART_USB_1
    UART_USB_1 <--> |"USB"| USB_CT1_1
    UART_USB_2 <--> |"USB"| USB_CT1_2
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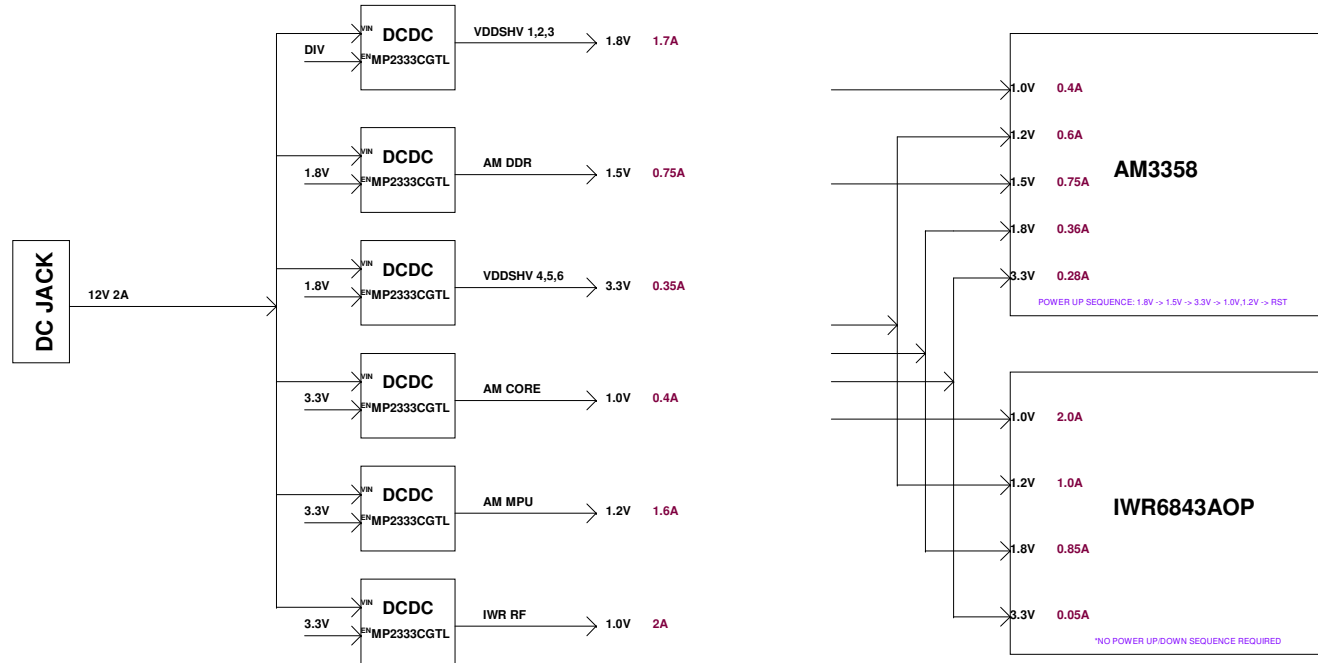
CAAYO

CAVECSSCH00E00


CAAYO		CAVECSSCH00E00	
Designer Yash		Size C	Scale 1:1
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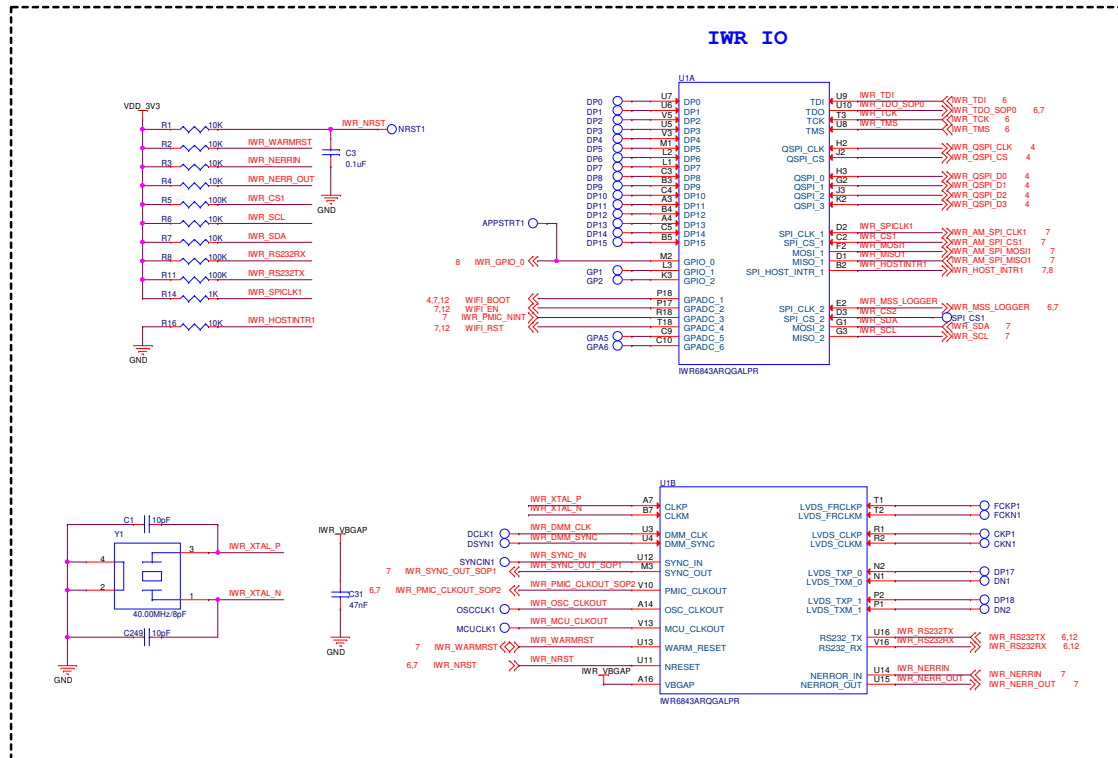
POWER TREE



<Variant Name>

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	Drawing Title POWER TREE			
Designer Yash	Size C	Scale	Document Number CAVECSSCH00E00	Rev 0.1
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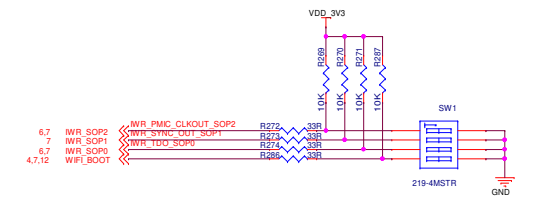
IWR IO



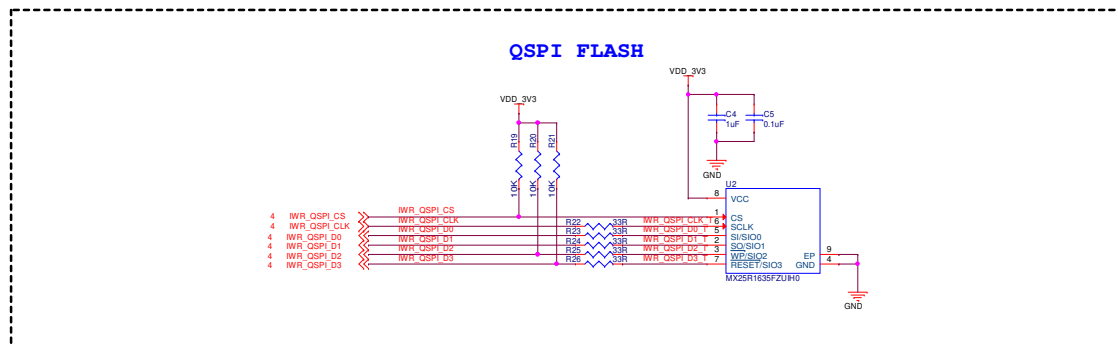
SOP MODE

SOP2 (P9)	SOP1 (G13)	SOP0 (N13)	Bootloader Mode and Operation
0	0	1	Functional mode The device bootloader loads the user application from the QSPI serial flash to the internal RAM and switches the control to it.
1	0	1	Flashing mode The device bootloader spins in loop to allow flashing of the user application (or the device firmware patch – supplied by TI).
0	1	1	Debug mode The bootloader is bypassed and the R4F processor is halted. This lets the user connect the emulator at a known point.

SOP SELECTION



QSPI FLASH



<Variant Name>

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Date: Monday, September 13, 2021

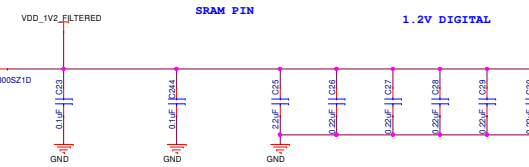
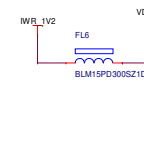
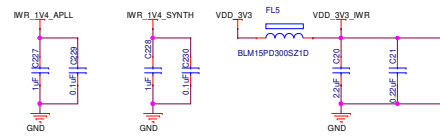
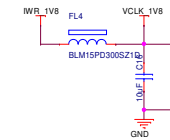
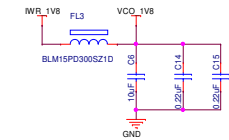
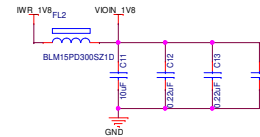
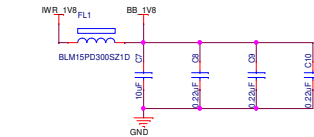
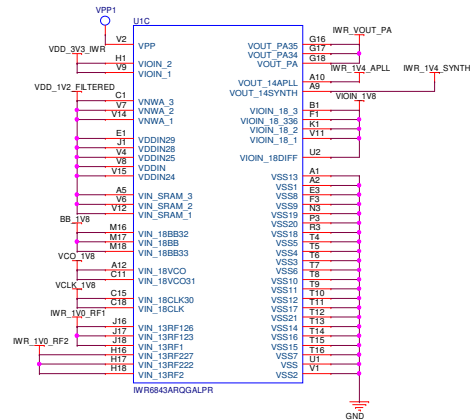
Rev 0.1
Sheet

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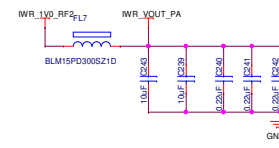
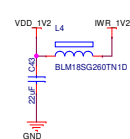
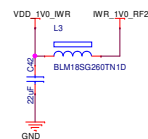
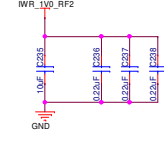
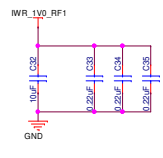
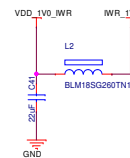
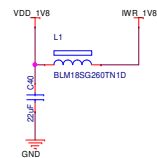
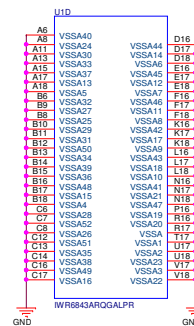
IWR POWER

DECOUPLING CAPS



- Do we need LDO BYPASS circuit for 1.2V and 1.8V?
- We are using BLM15PD300SZ1D bead.

LDO BYPASS

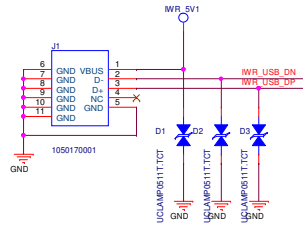


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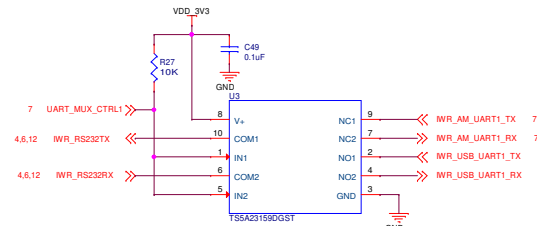
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IWR DEBUG

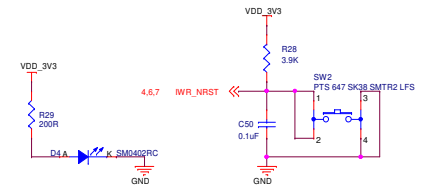
USB DEBUG



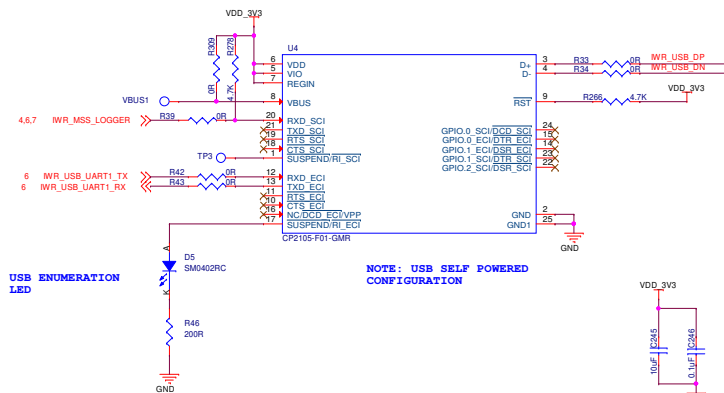
UART SELECTION



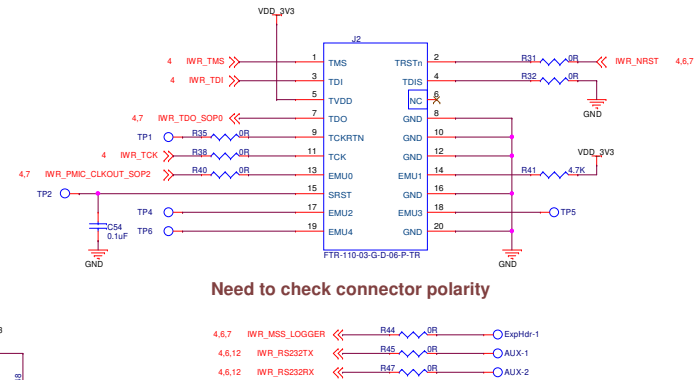
POWER LED & Reset Button



USB UARTx2



JTAG CTI20



Need to check connector polarity

<Variant Name>

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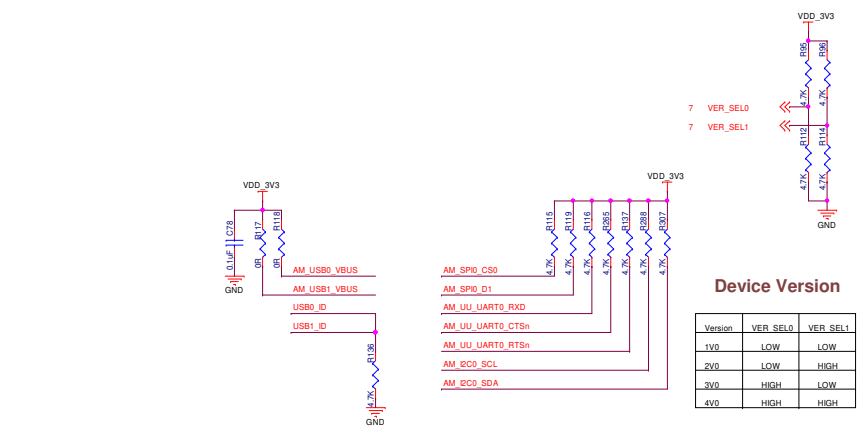
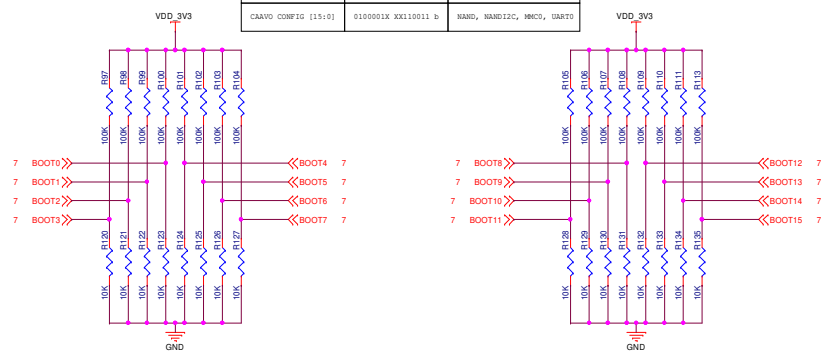
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AM IO



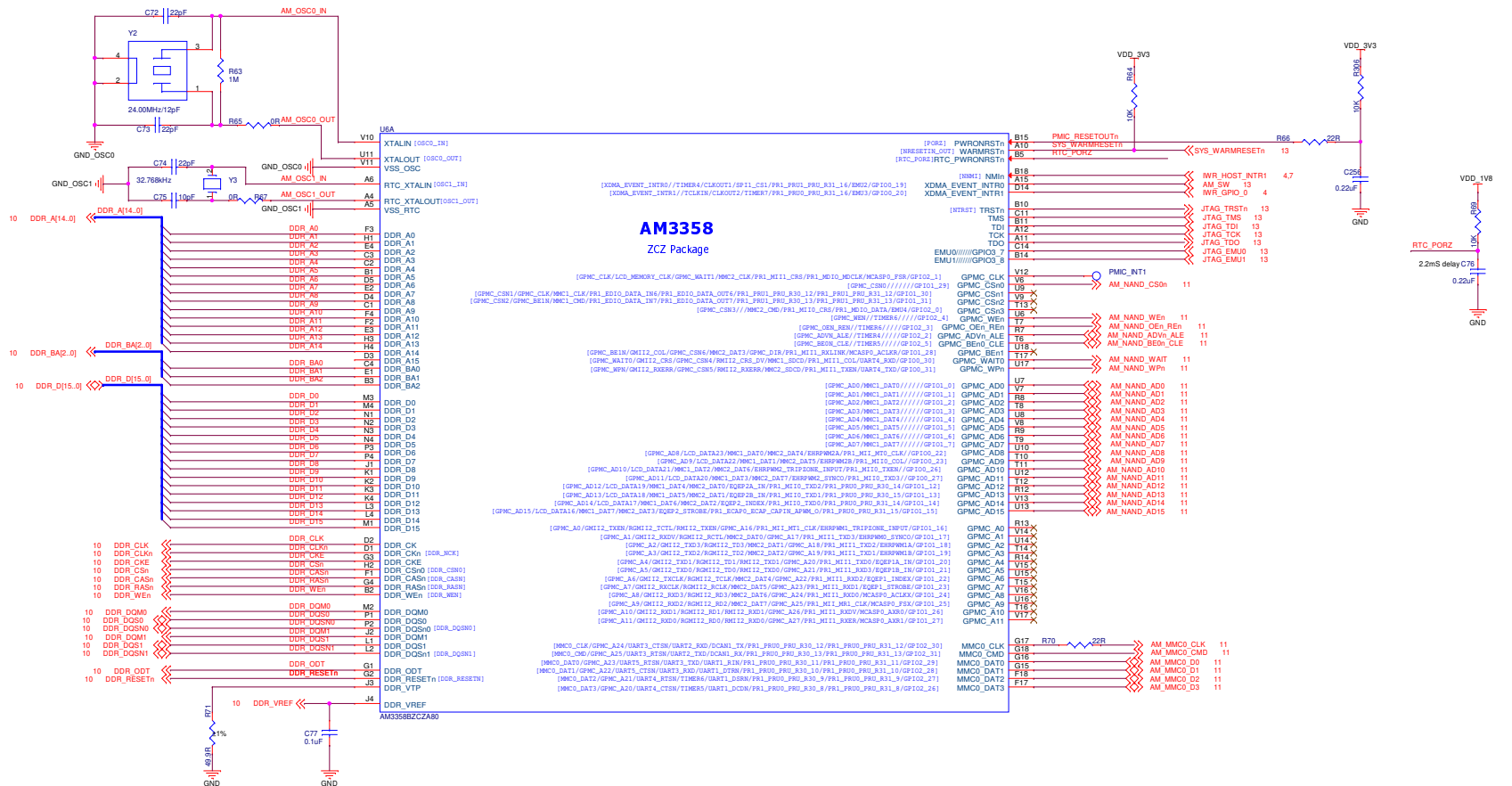
Boot Configuration

EVM CONFIG [15:0]	0100XXXXXXXX110111b	MMC0, SPI0, UART0, USB0
CAAVO CONFIG [15:0]	0100001X XX110011 b	NAND, NANDI2C, MMC0, UART0



Version	VER_SEL0	VER_SEL1
1V0	LOW	LOW
2V0	LOW	HIGH
3V0	HIGH	LOW
4V0	HIGH	HIGH

Do we need to connect GND_OSCx to Board Ground? As per datasheet we have to but in EVM Schematic it is not connected with Board GND



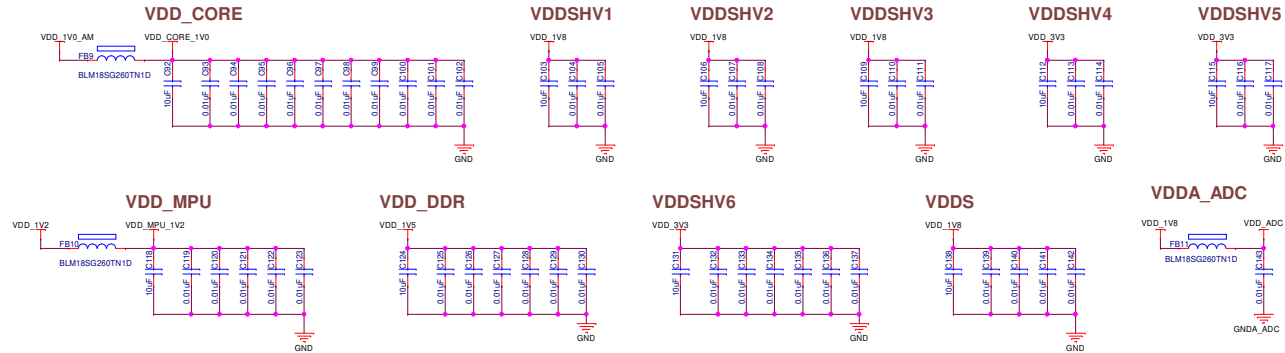
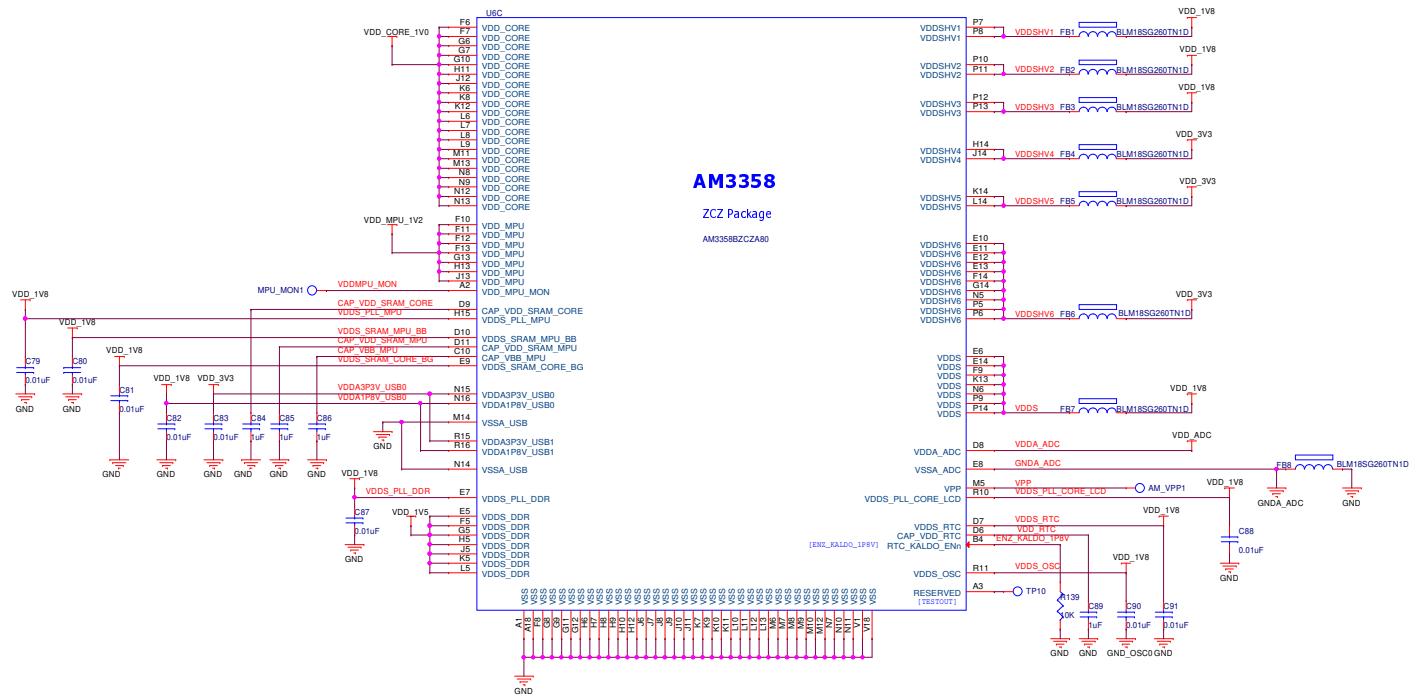
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	Title
	AM DDR FLASH

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AM POWER

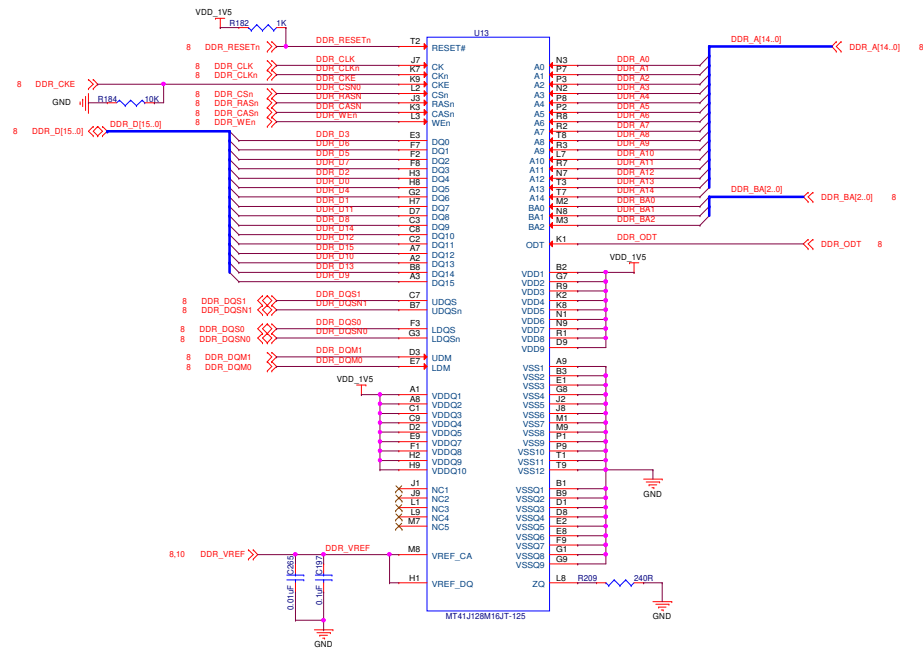


1.8V	3.3
vddshw1	vddshw4
vddshw2	vddshw5
vddshw3	vddshw6
vdds_osc	
vdds_rtc	
vddsx - ALL	

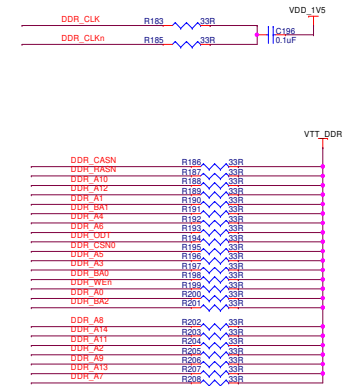
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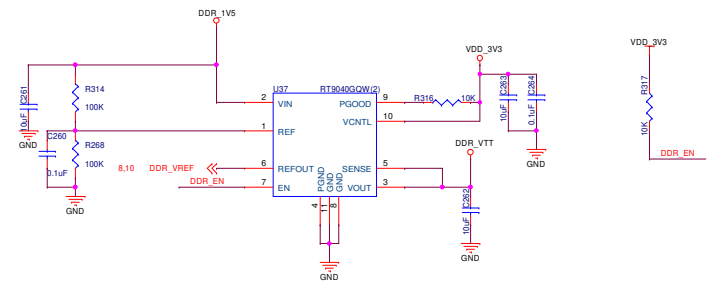
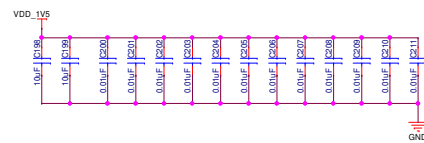
DDR MEMORY



Terminations



Power for DDR3 Terminators 0.75V/1.8A



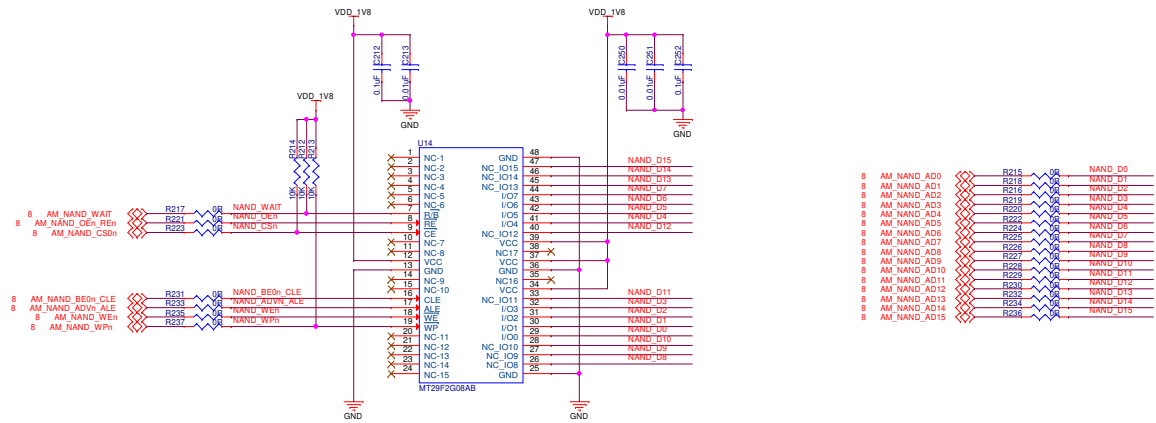
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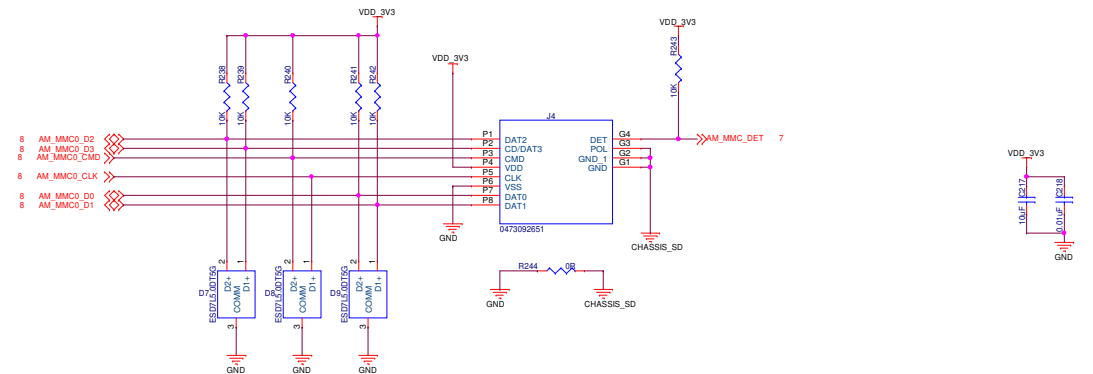
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NAND MMC

NAND MEMORY



SD CARD



<Variant Name>

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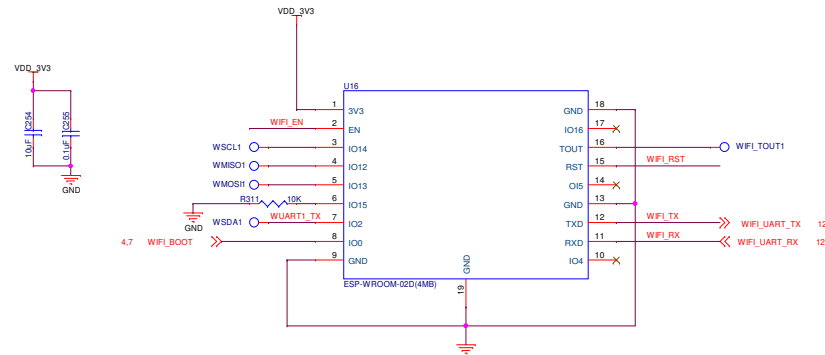
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Title
NAND MMC

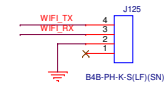
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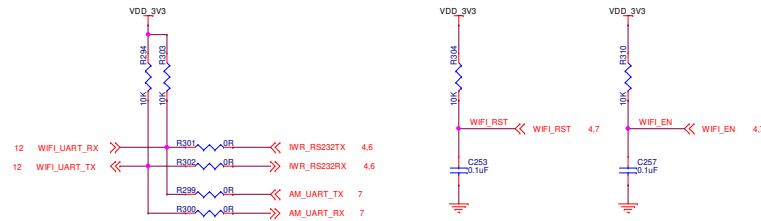
WIFI



FLASH CONNECTOR



UART SELECTION



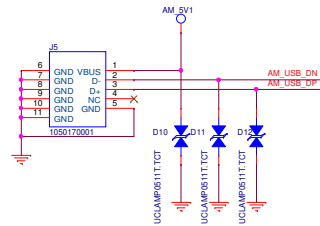
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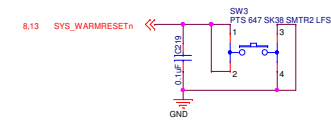
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AM DEBUG

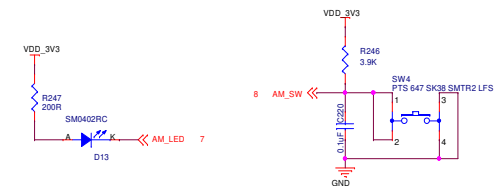
USB DEBUG



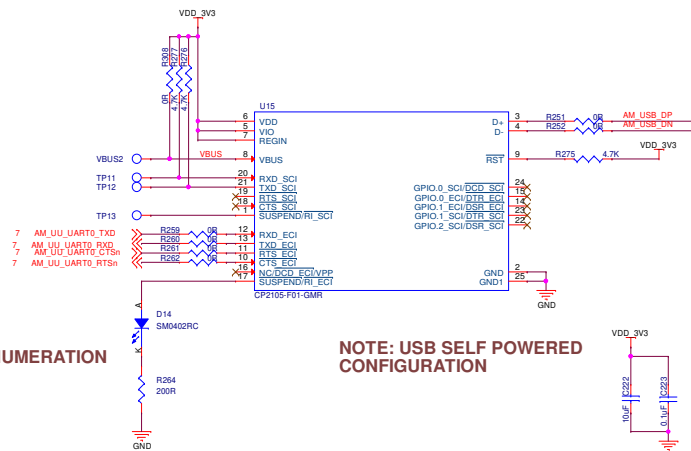
Reset Button



MULTI PURPOSE LED & BUTTON



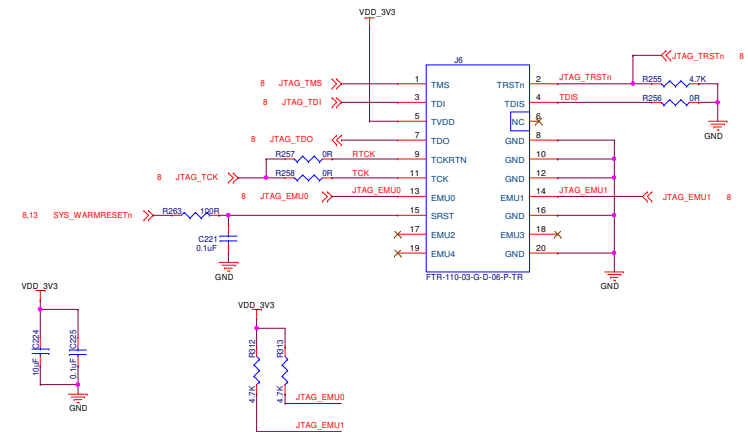
USB UART



USB ENUMERATION LED

NOTE: USB SELF POWERED CONFIGURATION

JTAG

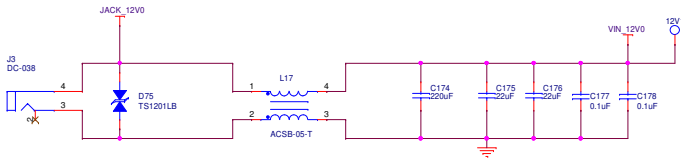


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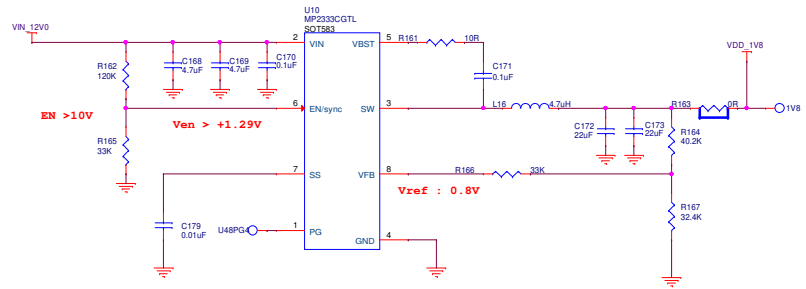
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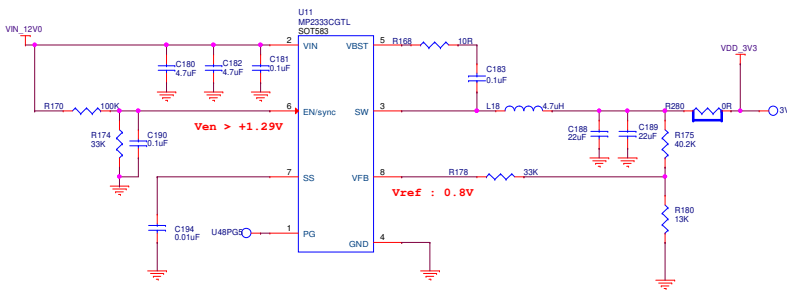
12V Power Input



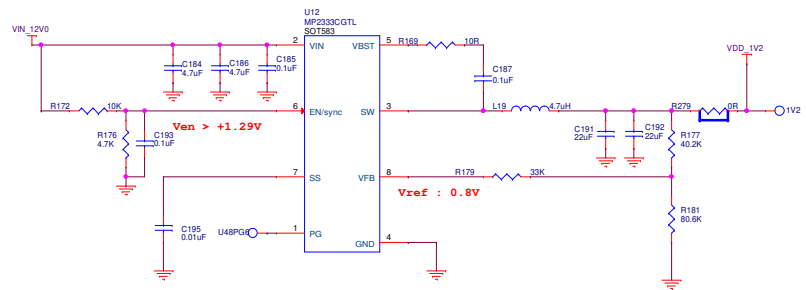
IWR AM 1V8/2A



IWR AM 3V3/0.5A



AM IWR 1V2/2A

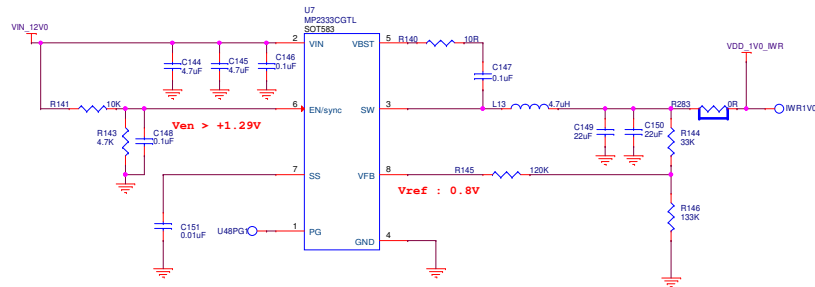


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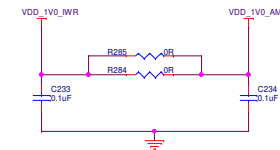
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DCDC - INDIVIDUAL

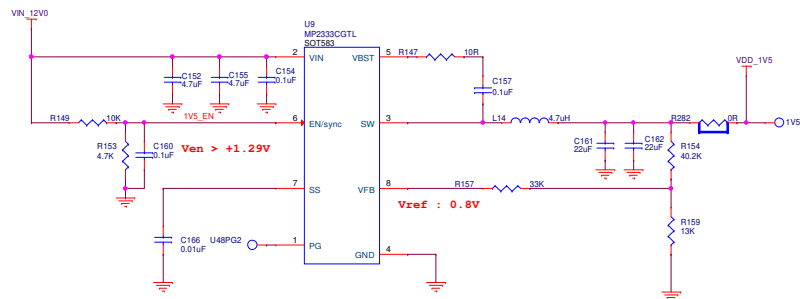
IWR RF 1V0/2A



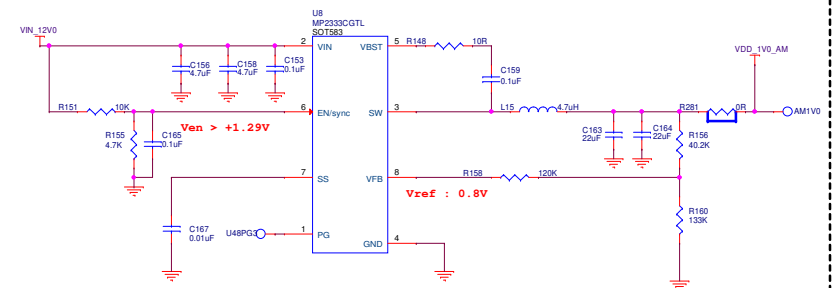
IWR AM 1V0/2.5A



AM DDR 1V5/1A



AM CORE 1V0/0.5A



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REVISION HISTORY

Rev#	Date	Originator(s)	Rev Item ID	What Revised	Why Revised	Rework# Base On Previous Version
0.1	17052018	Yash	1	Initial schematic with AM SoC & IWR		

<Variant Name>

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C	CAVESSCH-0000	0.1	REVISION HISTORY
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